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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,648	12/31/2001	Howard S. David	42390.P12981	9206

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,648	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/24/2004 has been entered.

Response to Amendment

2. This Office action is in response to the amendment field on 08/24/2004.

Specification

3. The disclosure is objected to because of the following informalities:

Page 5 lines 3-4, "the interconnect 265 may include 8 differential pairs, 9 pairs for data, and 9 pairs for address and command." should be -- the interconnect 265 may include 18 differential pairs, 9 pairs for data, and 9 pairs for address and command.--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

5. Regarding claim 1, Stracovsky discloses an apparatus, i.e., system (100, figure 1B) comprising an array of tag address storage locations, i.e., resource tags (114, figure 1B), and a command sequencer and serializer unit, i.e., command sequencer (116, figure 1B), the command sequencer control a memory module, i.e., shared memory (108, figure 1B), the command sequencer and serializer unit to use a first plurality of address and command signals to generate a plurality of signals, i.e., singles from processor(s) (902, figure 9a) via the system bus (906, figure 9a) to be input to the memory module via a point-to-point interconnect between the command sequencer, i.e., embedded in the memory controller (904, figure 9a) as the same structure defined in figure 1d), wherein the plurality of signals is fewer in number than the first plurality of address and command signals, as defined in figure 9a and (col. 11 line 5 through col. 13 line 17). Stracovsky differs from the claimed invention in not specifically teaches a data cache located on a memory module. However, Saulsbury discloses a system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory module, as per

teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 2, Saulsbury discloses the apparatus further comprising a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules, i.e., each tag identifies the row in the corresponding memory bank 118, (col. 7 lines 41-61).

Regarding claims 3-4, Saulsbury discloses each of the plurality of arrays of tag address storage locations organized into a plurality of ways and 4 ways (col. 3 lines 54-63).

Regarding claims 5, Stracovsky discloses the plurality of signals including a plurality of command and address lines with the highly priority accessing value (col. 11 line 57 through col. 12 line 19).

Regarding claim 7, Stracovsky discloses a memory module, i.e., system shared memory (108) comprising a plurality of memory bank, i.e., device type 1 – device type N (figure 1C), the memory banks are controlled by commands delivered by a memory controller, i.e., universal controller (104, figure 1B) over a memory bus (220, figure 1B), the memory controller component including an array of tag address storage locations, i.e., resource tags (114, figure 1B), the memory controller component is not located on the memory module, i.e., memory controller arranged to act as a liaison between a processor and shared memory (figure 1 B and col. 6 line 21 through col. 7 line 55), and a command sequencer and serializer unit, i.e., command sequencer (116, figure 1d) located in the universal controller, to use a first plurality of address and command signals to generate a plurality of signals to be input to the memory device, wherein the plurality of signals is fewer in number than the fist plurality of address and

command signals, as defined in figure 9a and (col. 11 line 5 through col. 13 line 17). Stracovsky differs from the claimed invention in not specifically teaches a data cache coupled to the memory device wherein the data cache is located on the memory module. However, Saulsbury discloses a system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module of Stracovsky in having a data cache located on a memory module, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 8, Saulsbury discloses the apparatus further comprising a command decoder and the serializer, i.e., decoder (124, figure 2), to receive command and address information from the memory controller component, i.e., data cache bank control state machine (152) send out the W/R control commands and address (A20-A9) information via the bus 12 to the decoder (124), the command decoder and de-serializer unit providing control for the data cache, memory device (123, figure 2) provides requested address to the data cache storage (144).

Regarding claim 9, the limitations of the claim are rejected as the same reasons set forth in claims 3-4.

Regarding claim 10, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller, i.e., universal controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B), the memory controller including an array of tag address storage locations, i.e., resource tags (114, figure 1B), to use a first plurality

of address and command signals to generate a plurality of signals, wherein the plurality of signals is fewer in number than the fist plurality of address and command signals, i.e., singles from processor(s) (902, figure 9a) via the system bus (906, figure 9a) to be input to the memory module via a point-to-point interconnect between the command sequencer, i.e., embedded in the memory controller (904, figure 9a) as the same structure defined in figure 1d), wherein the plurality of signals is fewer in number than the first plurality of address and command signals, as defined in figure 9a and (col. 11 line 5 through col. 13 line 17), and a memory module, shared memory (108, figure 1B) separate from and coupled to the memory controller via a memory bus (220, figure 1B). Stracovsky differs from the claimed invention in not specifically teaches the memory module including a memory device, and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller. However, Saulsbury teaches in the computer system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), in addition, Saulsbury teaches the memory controller is able to accessing the data from the data cache memory via the primary data cache bank logic (150, figure 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory device of Stracovsky in having a memory device, and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 13, Saulsbury discloses the system further comprising a plurality of memory modules, i.e., memory block (104, figure 1), each of the plurality memory modules including at least one of a plurality of memory devices, i.e., main memory bank (118, figure 1) and one of a plurality of data caches, i.e., primary data cache (122, figure 1), each of the data caches controlled by commands delivered by the memory controller, i.e., CPU (102, figure 1).

Regarding claim 14, Saulsbury discloses the plurality of arrays of tag address storage locations and the plurality of data caches organized into four ways (col. 3 lines 54-63).

Regarding claim 15, Stracovsky discloses a method comprising receiving a read request at a memory controller (104, figure 1B) from processor(s) via the system bus (906, figure 9a), wherein the memory controller comprising a command sequencer and serializer unit, i.e., command sequencer (116, figure 1d), generating a plurality of signals from a first plurality of address and command signals using the command sequencer and serializer unit, wherein the plurality of signals is fewer in number than the first plurality of address and command signals, i.e., singles from processor(s) (902, figure 9a) via the system bus (906, figure 9a) to be input to the memory module via a point-to-point interconnect between the command sequencer, i.e., embedded in the memory controller (904, figure 9a) as the same structure defined in figure 1d), wherein the plurality of signals is fewer in number than the first plurality of address and command signals, as defined in figure 9a and (col. 11 line 5 through col. 13 line 17)performing a tag look-up with the memory controller to determine whether there is a hit for the read request in the memory (col. 7 line 25 through col. 8 line 2), fetching the data from the memory if the tag look-up indicates a hit, the memory module separate from the memory controller and coupled to the memory controller via a memory bus (220, figure 1B). Stracovsky differs from the claimed

invention in not specifically teaches the memory module including a data cache, the data cache controlled by commands delivered by the memory controller. However, Saulsbury teaches in the computer system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), in addition, Saulsbury teaches the memory controller is able to accessing the data from the data cache memory via the primary data cache bank logic (150, figure 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory device of Stracovsky in having a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 16, Saulsbury discloses the method further comprising loading a line of data from a memory device located on the memory module to the data cache if the tag look-up indicates a cache miss via the cache line bus (4096), and delivering the line of data to the memory controller (col. 11 line 59 through col. 12 line 2).

Response to Arguments

6. Applicant's arguments with respect to claims 1-5 and 7-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoo et al. (US Pub. 2002/0,129,215) disclosures memory system having point-to-point bus configuation (abstract).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

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